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Acquisition and control command system for power pulsed detectors

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ABSTRACT: A DAQ system is developed within the SiW-Ecal ILC collaboration. It provides a flexible and scalable architecture, compound of four parts. A detector interface (DIF) extracting data from front-end electronics and sending them as packets. Two levels of data concentration, control clock and fast command fanout. The two cards, named DCC and GDCC, use respectively FastEthernet and GigaEthernet. A software suite (named Calicoes) allows to control the DAQ and the detector chips and to acquire data from GigaEthernet. It also includes programs for decoding frontend readout to various formats, and also dispatching and aggregating data. Overall architecture, performance in test beam and prospects for use with hundreds of thousands channels are discussed.

KEYWORDS: Control and monitor systems online; Data acquisition circuits; Front-end electronics for detector readout; Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases)

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1 The SiW-Ecal and its DAQ

The SiW-Ecal [1] is an electromagnetic calorimeter for the detector of the future International Linear Collider (ILC). It is an imaging calorimeter for particle flow algorithm, allowing a very high granularity. It is based on silicon sensors (P-I-N diodes matrix) with a pixel size of 5.5 mm $\times$ 5.5 mm, read by the Omega Skiroc2 chip [3]. For ILC, it is considered to construct a 30 layers calorimeter including tungsten plates representing 24 times the radiation length (3.5 mm). As the granularity is very high, we expect 100 million channels reading the data. In order to handle such an impressive flow of data, we need to conceive a high performance DAQ (Data AcQuisition system), which is able to scale to the dimension of the detector. To achieve this goal, the DAQ is divided in four parts. The detector interface board (DIF) is reading data directly from the chips and formats their data stream in packets. These packets are aggregated by two level of aggregation electronic cards. The data concentrator card (DCC) aggregates data from the DIF to use fully the capacity of the FastEthernet on HDMI cable. The Giga concentrator card (GDCC) converts this streams to Giga-Ethernet encoding, upscaling to Gigabit/s. The acquisition clock and the detector-level commands are sent through a specific card named the Clock and Control Card (CCC) which converts the analogic signal into numeric words. These commands words are fanned-out by both GDCC and DCC to the DIF. A software suite, named Calicoes, handles the data acquisition and control-command of the whole system. A data acquisition chain acquires Gigabit data flow. It is able to dispatch this data through several kinds of media (files, shared memory and TCP socket). In real-time, it verifies the integrity of the data flow and extracts the data to produce physical events and feeds an event builder. The software suite includes also a complete control and command system, allowing to configure all the cards from a single XML configuration file.

Due to the expected beam structure on a future ILC, the whole detector can be put into a "suspend" state during collision free gaps. At the level of the very front-end chip this feature

is implemented by unbiasing the current sources of internal blocks (power supply voltage remains constant). The overall power consumption can be dramatically decreased by a factor 100. To ensure a proper functioning of several detector modules, the DAQ system features an isochronous path to every module in order to distribute the time controlled signals used to wake the detector up or put it into suspend mode. This fast control channel is interleaved with control data using some control characters provided by the 8b/10b encoding. The time precision is at the order of the bit clock (20 ns in the present implementation). A specific command is used to align clocks on modules. The DAQ system also includes several timers to sequence the wake-up sequence properly in three phases: current-on, acquisition start then enable triggers. This allows to avoid catching noise generated at wake-up. The major consequence for the DAQ system is the arrival of data packets in bursts. A specific buffering scheme with round-robin selectors has been implemented into the various firmwares. In addition fast control commands are also used for real-time control of the data throughput allowing each component to be put into a pause state waiting for buffer space to become available (to be tested). The actual power consumption is 60 μW/channel at 1% duty cycle (expected to be 25 μW/ch). Additional consumption can be explained by an increased power-on time which double the effective duty cycle on one hand and to a higher detector occupancy due to the test beam conditions.

2 The Detector Interface (DIF)

At front-end level, close to the detector a so called Detector Interface board (DIF) connects the detector modules to the control and DAQ system. While the shape of the DIF board can be adapted according to the constraint for the integration of each sub-detector, the firmware can be common to the ROC ASICs family from Omega team. The DIF is connected to the DAQ and control system using a customized 8b/10b serial link. All the functions are embedded in the same cable and same protocol: fast control, slow control (configuration) and data read-out. This link is synchronized using the beam clock ranging from 40 MHz to 120 MHz. For compatibility with test beam environment two other signals are distributed isochronously, an external trigger and a detector busy signal. Stringent height constraints have lead to choose HDMI standard as it can provide 5 differential pairs and some power connections within a rather small cross section. The same transceiver blocks (MAC layer) are used in every components of the system (firmware). The DIF prototypes (figure 1) are based on low cost FPGA and the room allocated to DIF in the current design is quite small, less than a credit card for connectors, power storage, regulators and buffers. A microchip, which could be shared with other detectors based on similar VFE chips, would be appropriate in order to integrate a simple SER/DES function, buffers and power management features. This chip could be power-pulsed an therefore could contribute to both power and room saving. The DIF architecture (figure 2) is versatile and extremely modular in order to make easier any update of functionalities. A specific internal bus is used in order to interconnect all the functions. It has a similar but lightweight architecture of a system on chip design with well separated communication ports, storage structure, peripherals (detector bus, external memory, ...) and a central supervisor (packet analysis, chip management, resource sharing, command handling, ...). A DIF board is expected to handle several thousands of detector channels. It allows to read and to write configuration memories, to send control orders and to receive acknowledges and finally to read physics data and

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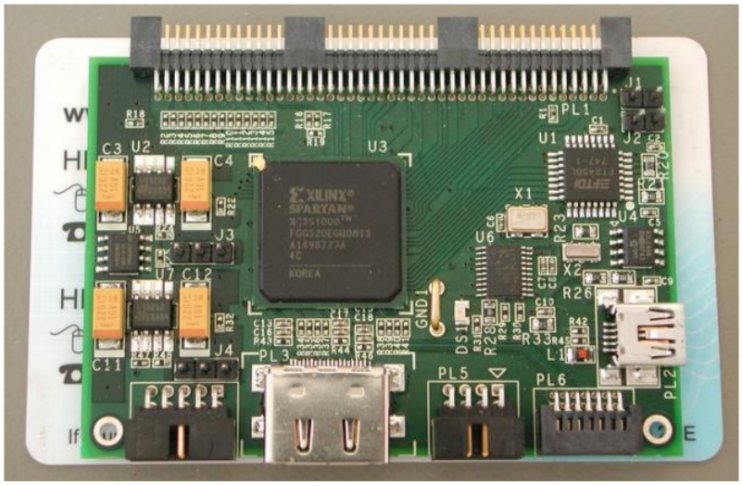

Figure 1. Picture of the DIF for the SiW-Ecal.

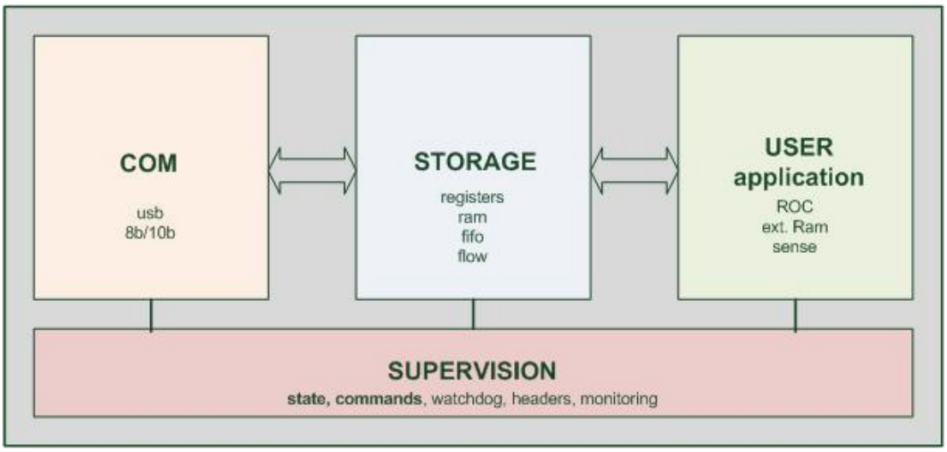

Figure 2. Simplified architecture of the DIF FPGA.

sent them through the DAQ system. Within the CALICE collaboration a DIF task force made up of 4 people is responsible for the specifications.

3 The DCC and GDCC

The GDCC (Gigabit Data Concentrator Card) board is an intermediate board in the DAQ system that allows several DIFs to be connected to a single PC. The downstream link is expected to work at 1 Gb/s. The upstream DIF links are expected to work at 50 Mb/s. The board (figure 3) is design on 6U VME format, and shared in 2 pieces, the main and the mezzanine. The main board contains all devices, the biggest if which is the FPGA XILINX Spartan XC6slx75. The mezzanine is equipped with the connectors for the upstream link.

The downstream link is based on standard protocol and the Ethernet physical connection is done either by a fiber SFP module or CAT5 copper. The Ethernet physical layer is done via a commercial device MARVELL 88E1111. This device support the Gigabit Media Independent Interface

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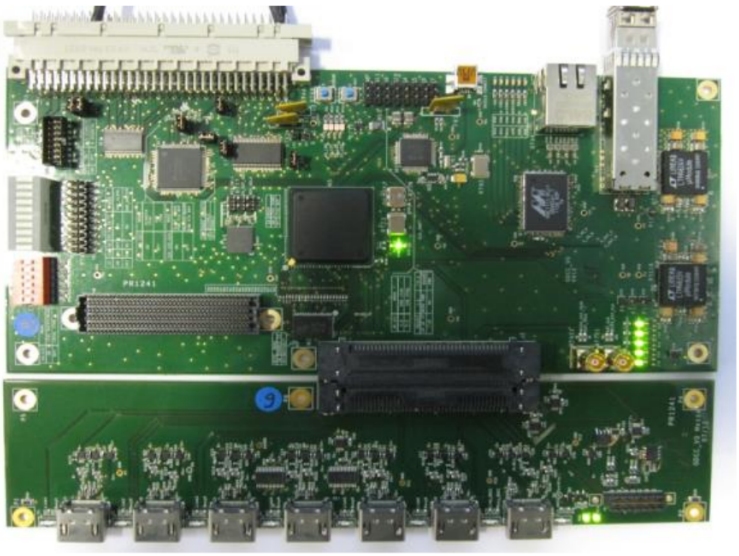

Figure 3. The GDCC Board.

for direct connection to a MAC block. It achieves robust performance in noisy environments with a very low dissipation. The power consumption of the board is approxymatively 5 W and here this is not critical for the DAQ usage. The power dissipation of the MARVELL component is 0,75 W, the idea about this specification is to try to group a range of components that could be a candidate for the next generation of board where the dissipation should be a challenge.

For the upstream link, it was decided to use commercial available cables with multiple LVDS links and the solution was to employ HDMI cables. On other side, it was decided to put in place these connectors on mezzanine board in order to follow the evolution of a new future connection if needed. The link is totally custom, and implemented in synchronous SERDES design inside the FPGA. The HDMI connector have five LVDS pairs, for our system we use only three pairs which are the data (DIF to GDCC), the control (GDCC to DIF) and the clock distributed from the CCC to all boards. The 2 extra pairs could be use for example for a trigger and busy signals.

The functionalities put in place in FPGA are only based on VHDL source (figure 4) shared by the ILC collaboration and few source references design from Xilinx web site.

The DCC (Data Concentrator Card) board allow to increase the number of DIF connection to a GDCC if needed. It can multiplex up to 9 DIF on a single HDMI cable. This board has the same behavior as a hub, the data rate on upstream is identical to the downstream, for our case, it is 50 Mb/s. The main specification for this board is to be connected or unconnected without changing the functionalities or the behavior on DAQ chain. To keep these compatibilities, we have decided to share the VHDL code with the neighbor board (DIF and GDCC). Thus, the DCC must be seen like a DIF from the GDCC and seen like a GDCC from the DIF. The board is a 6U VME format, it may be connected in VME Chassis to power-up it. The signals and connectors are also compatible with the DIF and GDCC and are based on HDMI.

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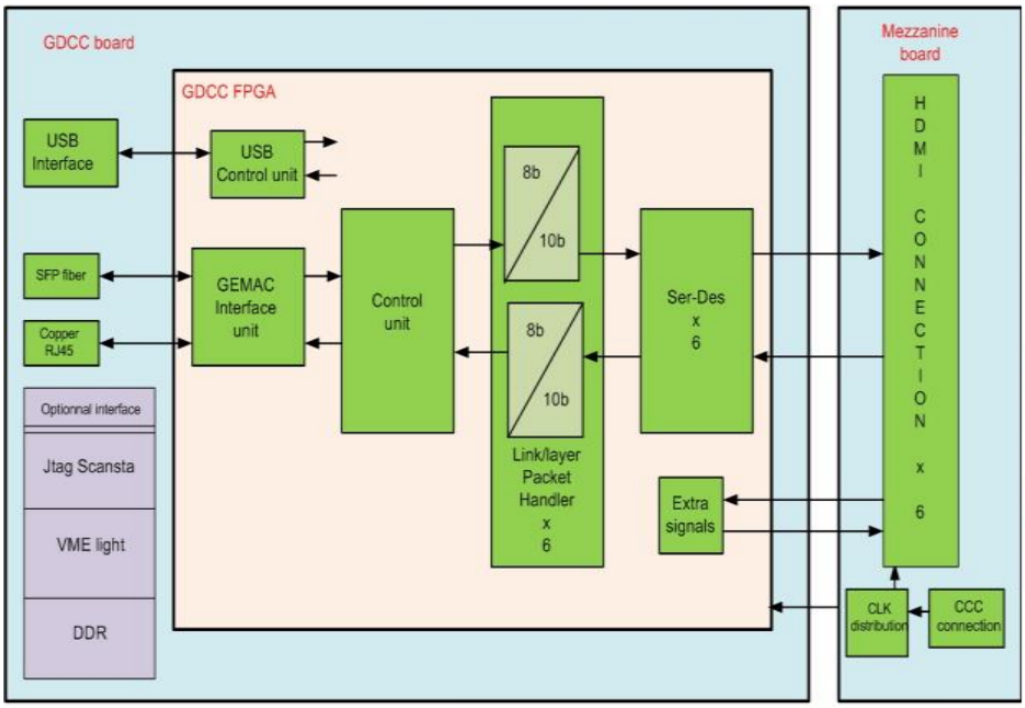

Figure 4. Architecture of the GDCC FPGA.

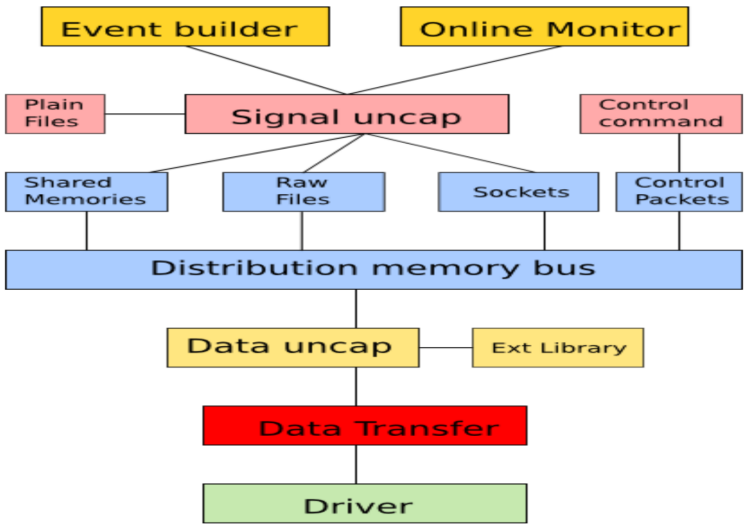

Figure 5. Acquisition chain, software architecture.

4 The acquisition chain

The acquisition chain is a set of software blocks communicating by shared memory or TCP sockets. Most of the blocks are generic and can be used for any kind of data and media. Some part, essentially the uncappers (data extraction blocks) are specific to the ROC ASICS. The figure 5 gives a global view of this acquisition chain.

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The driver and data transfer are the lowest level software blocks. They handle the reading of the data from the media. As we use a standard hardware to get network packets, we use a standard driver. The data transfer part is adapted to the nature of the stream. Until now, three adapters has been written: raw ethernet, UDP and file reading for replaying previous run (for debugguing purpose). Once the data is acquired, it is treated in the first uncapping block. This one is responsible for removing the network headers and trailers, verifying integrity and scheduling of the packets. The DIF specific part is implemented in an external library in order to let the core of the program totally generic. In this uncap block, the data are divided into streams, corresponding to the different parts of the detector.

This streams of data are then dispatched over the different programs that needs them. Three ways of getting them are proposed: shared memory for high performance local treatment, raw files for offline treatment and TCP sockets for low performance remote treatment. There is also a derivation to isolate the control packets and dispatch them in the control-command system.

Then the streams are sent to a signal uncapper, specialized for a type of ROC ASIC, it will transform the raw data into physical events. This uncapper provides plain text files as an output. It also provides statistics for technical studies.

This physicals events can then go through an event builder or an online monitor, which are outside the scope of this acquisition chain.

5 The control-command system

The control-command system is organised as a set of independent software blocks, linked by TCP sockets and XML connectivity description files.

Calicoes is based on an underlying framework named Pyrame, developped at LLR. Its command module is basically a Python virtual machine coupled with a TCP server and an XML parser. The simplicity of Python allows to develop very easily any new control-command and is stable enough for acquiring data during weeks. Pyrame also provides drivers for all the common bus and their encodings (Ethernet, GPIB, RS-232, LXI...). Finally, Pyrame is very open by the nature of its formats. One can address a Pyrame module by simply opening a TCP socket and sending an XML command. Thus, it is very easy to bind these control-command to any other existing framework. Actually, Pyrame has bindings for C/C++, Python and, R language but also for the Tango and the OPC-UA SCADA.

Based on this framework, a global control-command system has been written for the whole detector. It is based on basic blocks, linked together to build a complete system. The figure 6 describes the whole system. In the lower side, managing the hardware, we use the Pyrame bus blocks. On top of these, the electronics cards are driven by their own block, written in Python and running in a command module. As it would be too expensive in resource to run a module for every card, they are federated by a single module, managing all the similar cards. They are identified by a unique integer identifier. All the cards are federated by the acquisition PC control-command. This one is responsible for launching all the operation with the good scheduling.

On the top of all this, a detector level control-command allows the responsible of the experiment to drive the whole system as a black box, driven by a simple state machine (figure 7). This

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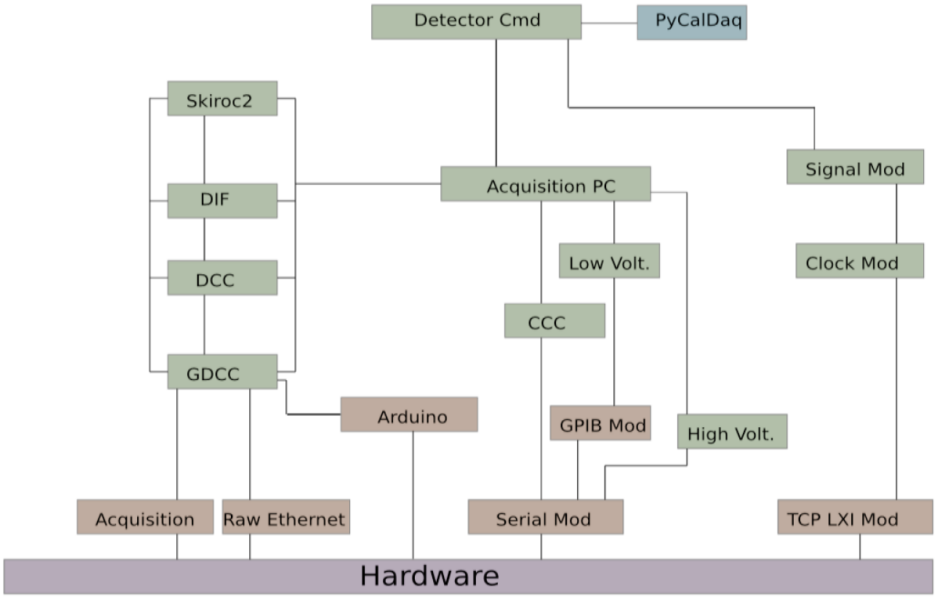

Figure 6. Global control-command architecture.

high level is also drivable by Pycaldaq which is a Python module for scripting the actions on the detector. This is really useful for calibration.

In order to configure such a complicated system, we developped a specific XML configuration file format allowing to describe easily the whole configuration of the system. The format includes several kind of implicit declaration giving a very compact format. A program reads this XML file and dispatch the parameters through all the control-commands modules. Then, the parameters are sent to the cards by all the modules in a sequential way.

6 Results

This DAQ has been used on the SiW-Ecal technical prototype for two years. It has been used successfully for 4 testbeams at DESY. The typical setup of these testbeams are composed of 10 layers of detection with their own DIF connected to 2 GDCCs. This configuration has generated approximatively 250 Gbytes of data, demonstrating the ability of the DAQ to take big amount of data. The system is validated for 10 Hz of spill frequency (ILC requirement is 5 Hz). The DIF and aggregating electronics and also the software can run at higher frequencies but at the chip level, some data can be corrupted if the frequency is higher than 10 Hz.

The system is globally stable. Some problems can occur at power-up like bad initialization of electronics. These problems can be overcomed by power-off/power-on routine. Once the system is in a running phase, it becomes stable and can accept lots of configuration without any problem. For example, we performed a channel by channel calibration, injecting 120000 configurations in the system in three weeks. The system remained totally stable during all this time.

The system is in a functional phase and produces good physical data, even in power-pulsed mode. We observe a typical signal over noise ratio of 15 which can be even better in continuous current with heavily filtered power supply and reduction of the channel number.

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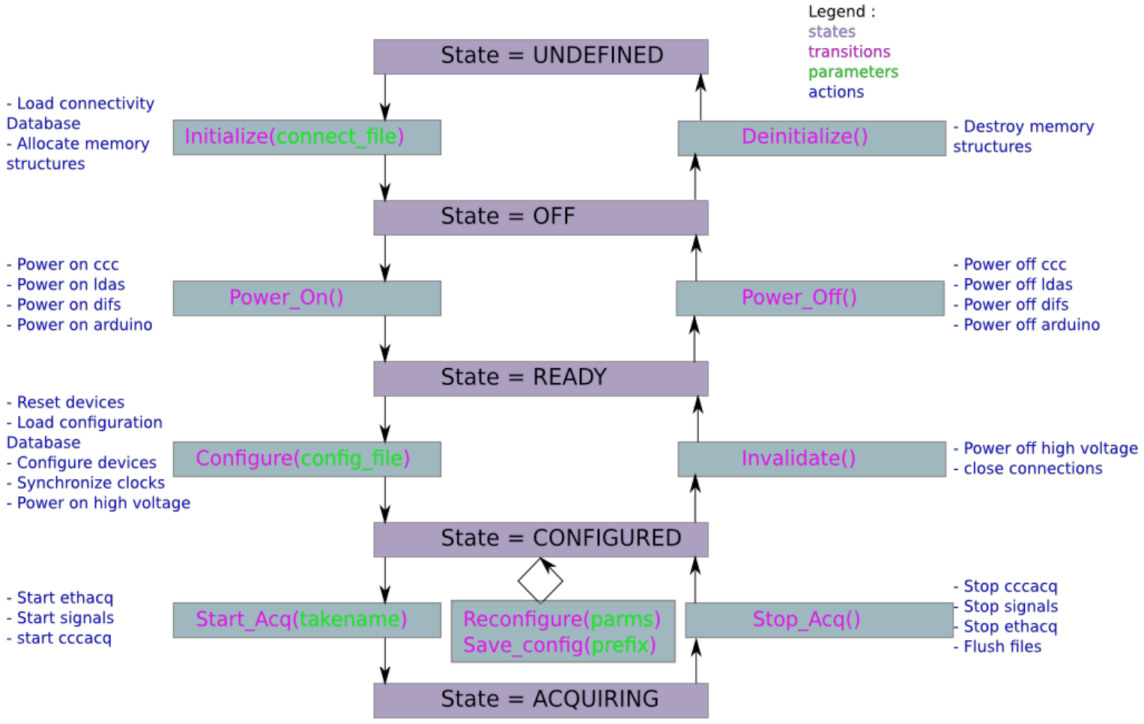

Figure 7. State machine of the detector control-command.

7 Perspectives

The system is a technical prototype working finely for our limited testbeam setup. In the context of the International Linear Collider Detector, the form factors should be optimized for fitting in the limited space and power consumption of the ECAL. In its actual form, the system, designed for a 100M-channels ECAL, should require 12500 DCC, 2000 GDCC and 200 acquisition PC.

For reducing the big number of cards, we are now working on smaller frontend modules for easyness of integration in the very thin layers of the ECAL. On the other hand, we are working for integrating all the computation components on the top module (in the space between the ECAL and the HCAL).

The software modularity induces a highly parallelisable context, but in order to reduce the size of the acquisition cluster, we are studying possibilities to integrate acquisition and uncapping software in many-core cards.

Acknowledgments

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